

## Ultra-low Quiescent Current ( $I_Q = 0.3 \mu A$ ), 300 mA, Buck-Boost DC/DC Converter

No. EA-415-210709

### OVERVIEW

The RP604x is a buck-boost converter featuring a minimum supply current and a high efficiency at low-load. The device operates at the low operating quiescent current ( $I_Q = 0.3 \mu A$ ) to make the most of battery life for the battery driver operated intermittently.

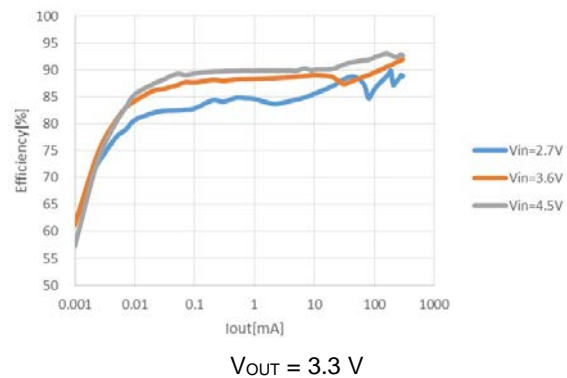
### KEY BENEFITS

- The low supply current ( $I_Q = 0.3 \mu A$ ) can achieve making battery life longer and battery's size-reduction.
- Wide range of input voltage (1.8 V to 5.5 V) can support for every battery from a coin-type battery to a USB port.
- Selectable package: WLCSP-20-P2 or DFN(PLP)2730-12

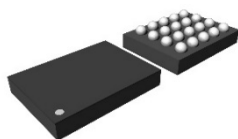
### KEY SPECIFICATIONS

- Input Voltage: 1.8 V to 5.5 V
- Output Voltage: 1.6 V to 5.2 V, 0.1 V step
- Output Voltage Accuracy:  $\pm 1.5\%$
- Maximum Output Current: 300 mA at Buck
- Built-in Driver On-resistance (RP604Z,  $V_{IN} = 3.6 V$ ): PMOS = Typ. 0.12  $\Omega$ , NMOS = Typ. 0.12  $\Omega$
- Operating Quiescent Current ( $I_Q$ ): 0.3  $\mu A$
- Standby Current: 0.01  $\mu A$
- Protection Features: UVLO, OVP, LX Peak Current, and Thermal Shutdown

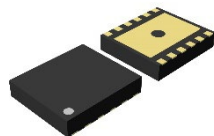
### TYPICAL CHARACTERISTICS



### PACKAGES



**WLCSP-20-P2**  
1.71 x 2.315 x 0.40<sup>(1)</sup> mm  
(<sup>1</sup>) maximum dimension



**DFN(PLP)2730-12**  
2.70 x 3.00 x 0.6<sup>(1)</sup> mm  
(<sup>1</sup>) maximum dimension

### OPTIONAL FUNCTIONS

The auto-discharge function and the set output voltage ( $V_{SET}$ ) are user-selectable options.

Product Name	Auto-discharge Function	$V_{SET}$
RP604xxx1A	Disable	1.6 V to 5.2 V (0.1 V step)
RP604xxx1B	Enable	

### APPLICATIONS

- Wearable Appliances: SmartWatch, SmartBand, Healthcare
- Li-ion/Coin Battery-used Equipment
- Low-power Wireless Communication Equipment: *Bluetooth*® Low Energy, ZigBee, WiSunm, ANT
- Low-power Devices for CPU, Memory, Sensor Device, Energy Harvesting

## SELECTION GUIDE

The set output voltage, the auto-discharge function<sup>(1)</sup> and the package are user-selectable options.

### Selection Guide

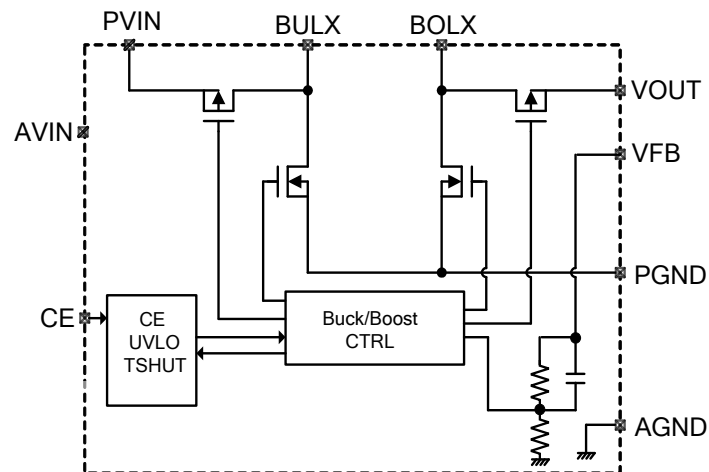
Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
RP604Zxx1\$-E2-F	WLCSP-20-P2	5,000 pcs	Yes	Yes
RP604Kxx1\$-TR	DFN(PLP)2730-12	5,000 pcs	Yes	Yes

xx: Specify the set output voltage ( $V_{SET}$ ) within the range of 1.6 V (16) to 5.2 V (52) in 0.1 V steps.

\$: Specify the auto-discharge function.

Version	Auto-discharge Function	$V_{SET}$
A	Disable	1.6 V to 5.2 V
B	Enable	

## BLOCK DIAGRAM



**RP604xxx1A/ RP604xxx1B Block Diagram**

<sup>(1)</sup> Auto-discharge function quickly lowers the output voltage to 0 V, when the chip enable signal is switched from the active mode to the standby mode, by releasing the electrical charge accumulated in the external capacitor.

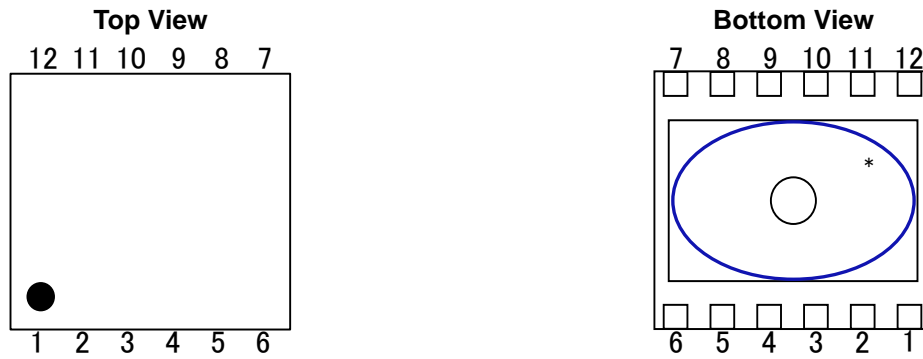
## PIN DESCRIPTIONS



WLCSP-20-P2 Pin Configuration

### WLCSP-20-P2 Pin Description

Pin No.	Pin Name	Description
A5, B5, C5	VOUT	Output Voltage Pin
A4, B4, C4	BOLX	Boost Switching Output Pin
A3, B3, C3, D3	PGND	Power GND Pin
A2, B2, C2	BULX	Buck Switching Output Pin
A1, B1, C1	PVIN	Power Input Voltage Pin
D1	AVIN	Analog Power Input Voltage Pin
D2	CE	Chip Enable Pin, Active-high
D4	AGND	Analog GND Pin
D5	VFB	Output Voltage Feedback Pin



DFN(PLP)2730-12 Pin Configuration

DFN(PLP)2730-12 Pin Description

Pin No.	Pin Name	Description
1	AVIN	Analog Power Input Voltage Pin
2	CE	Chip Enable Pin, Active-high
3	PGND	Power GND Pin
4	PGND	Power GND Pin
5	AGND	Analog GND Pin
6	VFB	Output Voltage Feedback Pin
7	VOUT	Output Voltage Pin
8	BOLX	Boost Switching Output Pin
9	PGND	Power GND Pin
10	PGND	Power GND Pin
11	BULX	Buck Switching Output Pin
12	PVIN	Power Input Voltage Pin

\* The tab on the bottom of the package shown by blue circle is a substrate potential (GND). It is recommended that this tab be connected to the ground plane on the board but it is possible to leave the tab floating.

## ABSOLUTE MAXIMUM RATINGS

**Absolute Maximum Ratings** (GND = 0 V)

Symbol	Parameter		Rating	Unit	
V <sub>IN</sub>	A/PVIN Pin Voltage		-0.3 to 6.5	V	
V <sub>BULX</sub>	BULX Pin Voltage		-0.3 to V <sub>IN</sub> + 0.3	V	
V <sub>BOLX</sub>	BOLX Pin Voltage		-0.3 to V <sub>OUT</sub> + 0.3	V	
V <sub>CE</sub>	CE Pin Voltage		-0.3 to 6.5	V	
V <sub>OUT</sub>	VOUT Pin Voltage		-0.3 to 6.5	V	
V <sub>FB</sub>	VFB Pin Voltage		-0.3 to 6.5	V	
I <sub>LX</sub>	BULX/BOLX Pin Output Current		900	mA	
P <sub>D</sub>	Power Dissipation <sup>(1)</sup>	WLCSP-20-P2	JEDEC STD. 51-9	1490	mW
		DFN(PLP)2730-12	JEDEC STD. 51-7	3100	mW
T <sub>j</sub>	Junction Temperature Range		-40 to 125	°C	
T <sub>stg</sub>	Storage Temperature Range		-55 to 125	°C	

### ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the life time and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings are not assured.

## RECOMMENDED OPERATING CONDITIONS

**Recommended Operating Conditions**

Symbol	Parameter	Rating	Unit
V <sub>IN</sub>	Input Voltage	1.8 to 5.5	V
T <sub>a</sub>	Operating Temperature Range	-40 to 85	°C

### RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

<sup>(1)</sup> Refer to *POWER DISSIPATION* for detailed information.

## ELECTRICAL CHARACTERISTICS

The specifications surrounded by   are guaranteed by design engineering at  $-40^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$ .

### RP604Z/K Electrical Characteristics

( $T_a = 25^{\circ}\text{C}$ )

Symbol	Parameter	Test Conditions/Comments	Min.	Typ.	Max.	Unit
$V_{\text{OUT}}$	Output Voltage	$V_{\text{IN}} = V_{\text{CE}} = 3.6 \text{ V}$	x 0.985		x 1.015	V
$I_{\text{Q}}$	Operating Quiescent Current	$V_{\text{IN}} = V_{\text{CE}} = V_{\text{OUT}} = 3.6 \text{ V}$ , $V_{\text{SET}} = 3.3\text{V}$ at rest		0.3		$\mu\text{A}$
$I_{\text{STANDBY}}$	Standby Current	$V_{\text{IN}} = 5.5 \text{ V}$ , $V_{\text{CE}} = 0 \text{ V}$		0.01	1	$\mu\text{A}$
$I_{\text{CEH}}$	CE Pin Input Current, High	$V_{\text{IN}} = V_{\text{CE}} = 5.5 \text{ V}$	<span style="border: 1px solid black; padding: 0 2px;">-0.025</span>	0	<span style="border: 1px solid black; padding: 0 2px;">0.025</span>	$\mu\text{A}$
$I_{\text{CEL}}$	CE Pin Input Current, Low	$V_{\text{IN}} = 5.5 \text{ V}$ , $V_{\text{CE}} = 0 \text{ V}$	<span style="border: 1px solid black; padding: 0 2px;">-0.025</span>	0	<span style="border: 1px solid black; padding: 0 2px;">0.025</span>	$\mu\text{A}$
$I_{\text{VOUTH}}$	VFB Pin Input Current, High	$V_{\text{IN}} = V_{\text{FB}} = 5.5 \text{ V}$ , $V_{\text{CE}} = 0 \text{ V}$	<span style="border: 1px solid black; padding: 0 2px;">-0.025</span>	0	<span style="border: 1px solid black; padding: 0 2px;">0.025</span>	$\mu\text{A}$
$I_{\text{VOUTL}}$	VFB Pin Input Current, Low	$V_{\text{IN}} = 5.5 \text{ V}$ , $V_{\text{CE}} = V_{\text{FB}} = 0 \text{ V}$	<span style="border: 1px solid black; padding: 0 2px;">-0.025</span>	0	<span style="border: 1px solid black; padding: 0 2px;">0.025</span>	$\mu\text{A}$
$V_{\text{OVP}}$	OVP Threshold Voltage	$V_{\text{IN}} = 3.6 \text{ V}$ , rising (detection)		6.0		V
		$V_{\text{IN}} = 3.6 \text{ V}$ , falling (release)		5.5		V
$R_{\text{DISN}}$	Auto-discharge NMOS On-resistance <sup>(1)</sup>	$V_{\text{IN}} = 3.6 \text{ V}$ , $V_{\text{CE}} = 0 \text{ V}$		100		$\Omega$
$V_{\text{CEH}}$	CE Pin Input Voltage, High	$V_{\text{IN}} = 5.5 \text{ V}$	<span style="border: 1px solid black; padding: 0 2px;">1.0</span>			V
$V_{\text{CEL}}$	CE Pin Input Voltage, Low	$V_{\text{IN}} = 2.0 \text{ V}$			<span style="border: 1px solid black; padding: 0 2px;">0.4</span>	V
$R_{\text{ONP}}$	PMOS On-resistance	RP604Z $V_{\text{IN}} = 3.6 \text{ V}$ , $I_{\text{LX}} = -100 \text{ mA}$		0.12		$\Omega$
		RP604K $V_{\text{IN}} = 3.6 \text{ V}$ , $I_{\text{LX}} = -100 \text{ mA}$		0.15		$\Omega$
$R_{\text{ONN}}$	NMOS On-resistance	RP604Z $V_{\text{IN}} = 3.6 \text{ V}$ , $I_{\text{LX}} = -100 \text{ mA}$		0.12		$\Omega$
		RP604K $V_{\text{IN}} = 3.6 \text{ V}$ , $I_{\text{LX}} = -100 \text{ mA}$		0.15		$\Omega$
$T_{\text{TSD}}$	Thermal Shutdown Threshold Temperature	$T_{\text{j}}$ , rising (detection)		140		$^{\circ}\text{C}$
$T_{\text{TSR}}$		$T_{\text{j}}$ , falling (release)		100		$^{\circ}\text{C}$
$t_{\text{START}}$	Soft-start Time	$V_{\text{IN}} = V_{\text{CE}} = 3.6 \text{ V}$		20		ms
$I_{\text{LXLIM}}$	LX Current Limit	$V_{\text{IN}} = V_{\text{CE}} = 3.6 \text{ V}$	<span style="border: 1px solid black; padding: 0 2px;">600</span>	900		mA
$V_{\text{UVLOF}}$	UVLO Threshold Voltage	$V_{\text{IN}} = V_{\text{CE}}$ , falling (detection)	<span style="border: 1px solid black; padding: 0 2px;">1.40</span>	1.50	<span style="border: 1px solid black; padding: 0 2px;">1.65</span>	V
$V_{\text{UVLOR}}$		$V_{\text{IN}} = V_{\text{CE}}$ , rising (release)	<span style="border: 1px solid black; padding: 0 2px;">1.55</span>	1.65	<span style="border: 1px solid black; padding: 0 2px;">1.80</span>	V

All test items listed under Electrical Characteristics are done under the pulse load condition ( $T_{\text{j}} \approx T_a = 25^{\circ}\text{C}$ ). Unless otherwise noted, the test runs with "Open-loop Control" ( $\text{GND} = 0 \text{ V}$ ).

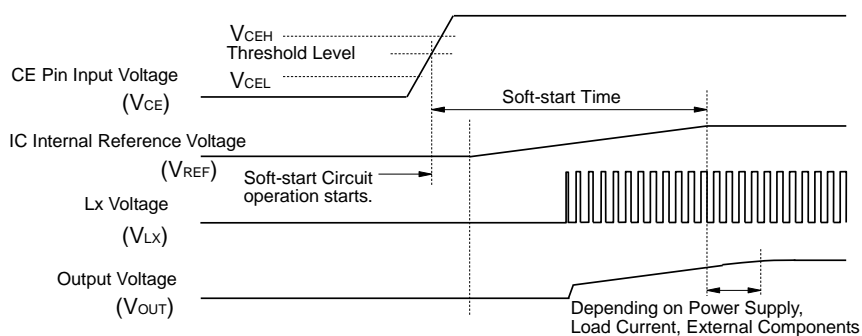
<sup>(1)</sup> RP604xxx1B only

## THEORY OF OPERATION

### Soft-start Time

#### Starting-up with CE Pin

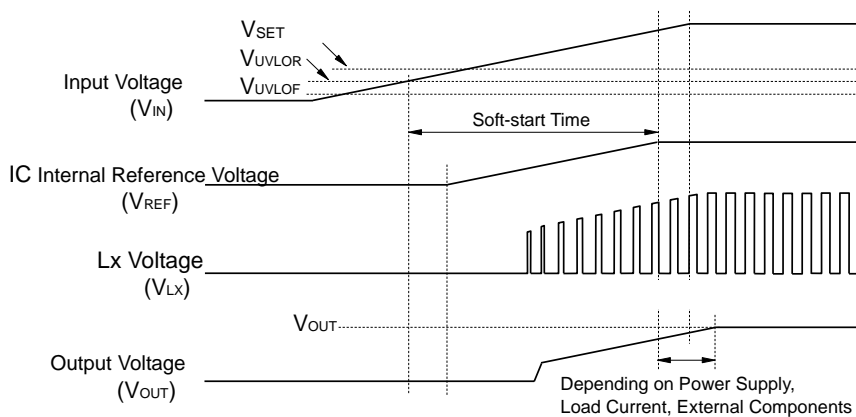
The IC starts to operate when the CE pin voltage ( $V_{CE}$ ) exceeds the threshold voltage. The threshold voltage is preset between CE "H" input voltage ( $V_{CEH}$ ) and CE "L" input voltage ( $V_{CEL}$ ). After the start-up of the IC, soft-start circuit starts to operate. Then, after a certain period of time, the reference voltage ( $V_{REF}$ ) in the IC gradually increases up to the specified value. Switching starts when  $V_{REF}$  reaches the preset voltage, and after that the output voltage rises accompanying  $V_{REF}$ 's increase. Soft-start time ( $t_{START}$ ) starts when soft-start circuit is activated, and ends when the reference voltage reaches the specified voltage. Soft start time is not always equal to the turn-on speed of the DC/DC converter. Note that the turn-on speed could be affected by the power supply capacity, the output current, the inductance value and the  $C_{OUT}$  value.



Timing Chart: Starting-up with CE Pin

#### Starting-up with Power Supply

After the power-on, when  $V_{IN}$  exceeds the UVLO released voltage ( $V_{UVLOR}$ ), the IC starts to operate. Then, soft-start circuit starts to operate and after a certain period of time,  $V_{REF}$  gradually increases up to the specified value. Switching starts when  $V_{REF}$  reaches the preset voltage, and after that the output voltage rises accompanying  $V_{REF}$ 's increase. Soft-start time starts when soft-start circuit is activated, and ends when  $V_{REF}$  reaches the specified voltage. Note that the turn-on speed of  $V_{OUT}$  could be affected by the power supply capacity, the output current, the inductance value, the  $C_{OUT}$  value and the turn-on speed of  $V_{IN}$  determined by  $C_{IN}$ .



Timing Chart: Starting-up with Power Supply

**Undervoltage Lockout (UVLO) Circuit**

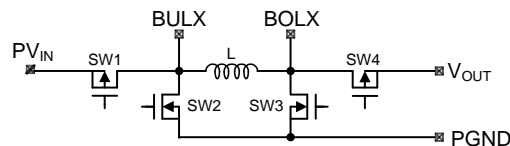
If the  $V_{IN}$  becomes lower than the UVLO detector threshold ( $V_{UVLOF}$ ), the UVLO circuit starts to operate,  $V_{REF}$  stops, and P-channel and N-channel built-in switch transistors turn "OFF". As a result,  $V_{OUT}$  drops according to the  $C_{OUT}$  capacitance value and the load. To restart the operation,  $V_{IN}$  needs to be higher than  $V_{UVLOR}$ .

**Overvoltage Protection (OVP) Circuit**

If the  $V_{OUT}$  becomes higher than the OVP detector threshold ( $V_{OVP}$ ), the OVP circuit starts to operate, P-channel and N-channel built-in switch transistors turn "OFF". As a result,  $V_{OUT}$  drops according to the  $C_{OUT}$  capacitance value and the load.

**Overcurrent Protection Circuit**

Overcurrent protection circuit supervises the inductor peak current (the peak current flowing through Pch Tr (SW1) in each switching cycle, and if the current exceeds the BULX current limit ( $I_{LXLIM}$ ), it turns off Pch Tr (SW1).  $I_{LXLIM}$  of the RP604x is set to Typ. 0.9 A.

**Simplified Diagram of Output Switches**

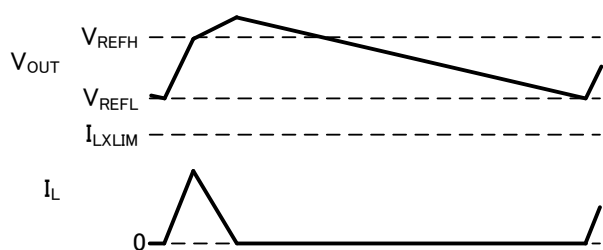


**VFM Mode**

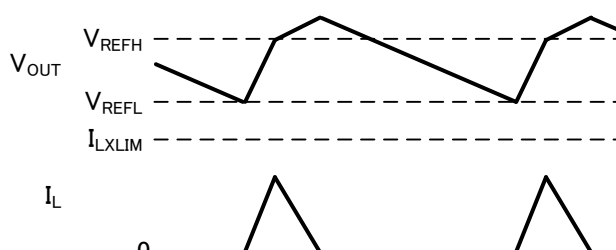
The VFM (Variable Frequency Modulation) mode is adopted as a switching method to achieve a high efficiency under light load conditions. A switching frequency varies depending on values of input voltage ( $V_{IN}$ ), output voltage ( $V_{OUT}$ ), and output current ( $I_{OUT}$ ). Check the actual characteristics to avoid the switching noise.

A switching starts when  $V_{OUT}$  drops below the lower-limit reference voltage ( $V_{REFL}$ ). When  $V_{OUT}$  exceeds the upper-limit reference voltage ( $V_{REFH}$ ), a constant voltage is output by a hysteresis control which stops the switching.

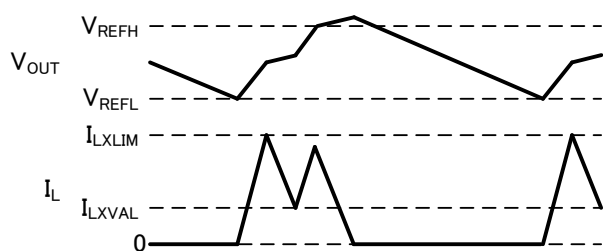
In order to operate within the rated characteristic of inductor and avoid the deteriorated band frequency of DC superimposed characteristics, when the inductor current ( $I_L$ ) exceeds LX current limit ( $I_{LXLIM}$ ), the operation shifts to off-cycle. And when  $I_L$  drops below the valley current limit ( $I_{LXVAL}$ ), the operation shifts to on-cycle.



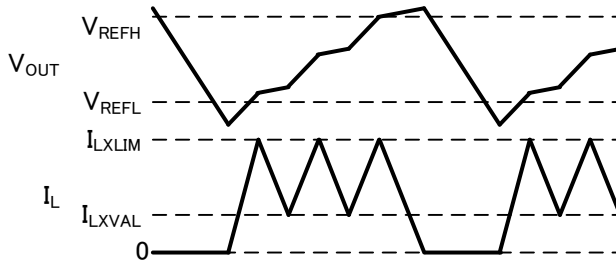
**No Load**



**Light Load**

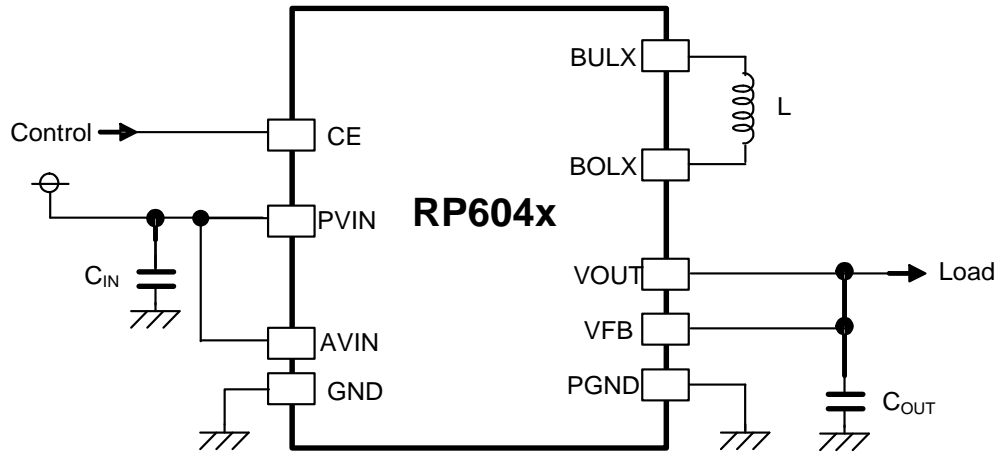


**Medium Load**



**Heavy Load**

**APPLICATION INFORMATION**



**RP604x Typical Application Circuit**

**Recommended External Components**

Symbol	Description
C <sub>IN</sub>	10 μF or more, Ceramic Capacitor
C <sub>OUT</sub>	22 μF, Ceramic Capacitor
L	2.2 μH, Inductor

## TECHNICAL NOTES

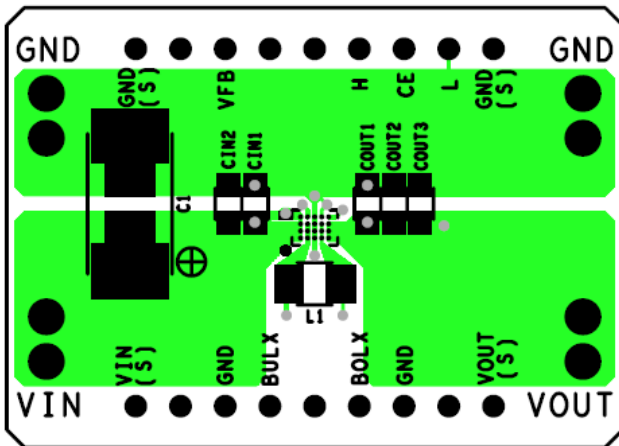
The performance of a power source circuit using this device is highly dependent on a peripheral circuit. A peripheral component or the device mounted on PCB should not exceed a rated voltage, a rated current or a rated power. When designing a peripheral circuit, please be fully aware of the following points. Refer to *PCB Layout* below.

- Use ceramic capacitors with a low equivalent series resistance (ESR), considering the bias characteristics and input/ output voltage.
- When the built-in switches are turned off, the inductor may generate a spike-shaped high voltage. Use the high-breakdown voltage capacitor ( $C_{OUT}$ ) which output voltage is 1.5 times or more than the set output voltage.
- Use an inductor that has a low DC resistance, has an enough tolerable current and is less likely to cause magnetic saturation. If the inductance value is extremely small, the peak current of  $L_X$  may increase. When the peak current of  $L_X$  reaches to the  $L_X$  limit current ( $I_{LXLIM}$ ), overcurrent protection circuit starts to operate. When selecting the inductor, consider the peak current of  $LX$  pin ( $I_{LXMAX}$ ).
- When an intermediate voltage other than  $V_{IN}$  or GND is input to the CE pin, a supply current may be increased with a through current of a logic circuit in the IC. The CE pin is neither pulled up nor pulled down, therefore an operation is not stable at open.

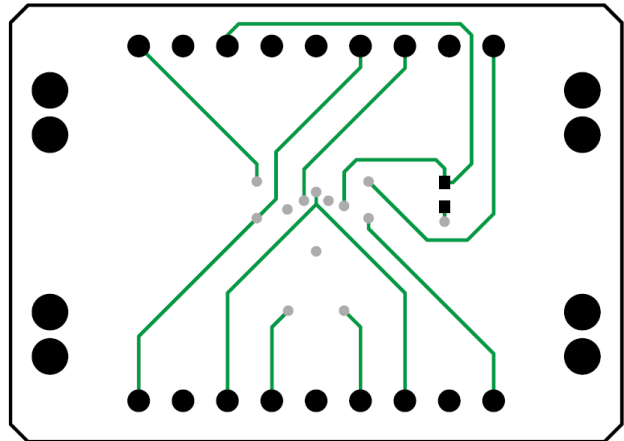
PCB Layout

RP604Z (Package: WLCSP-20-P2) PCB Layout

Topside

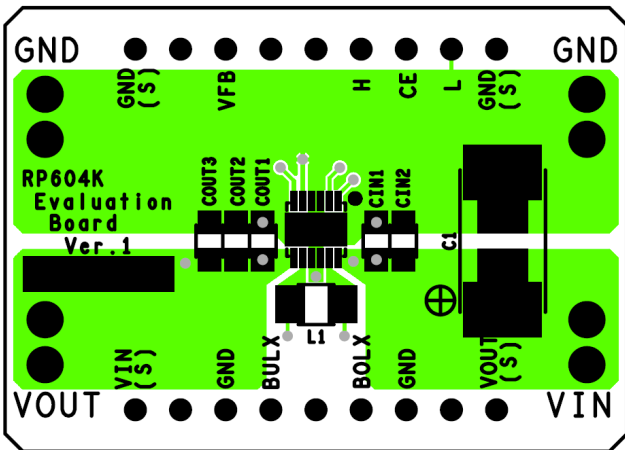


Backside

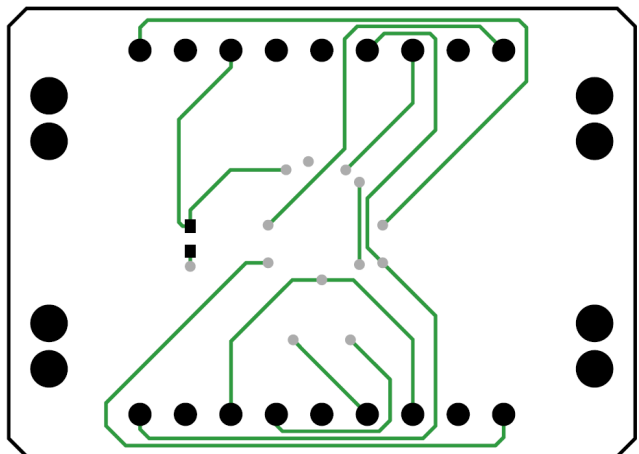


RP604K (Package: DFN(PLP)2730-12) PCB Layout

Topside



Backside

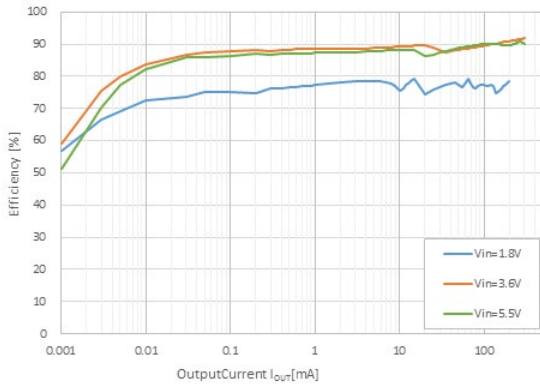


## TYPICAL CHARACTERISTICS

Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

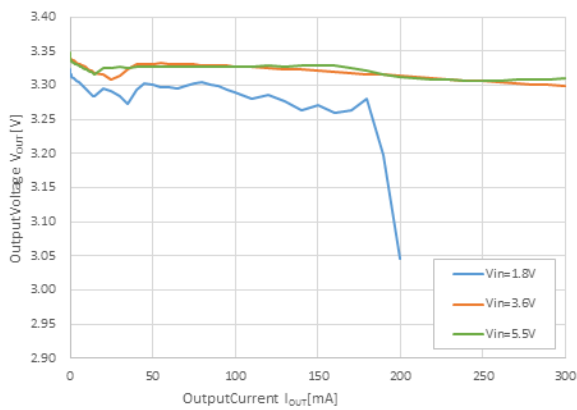
### 1) Output Current vs. Efficiency with Different Input Voltages

RP604Z331x



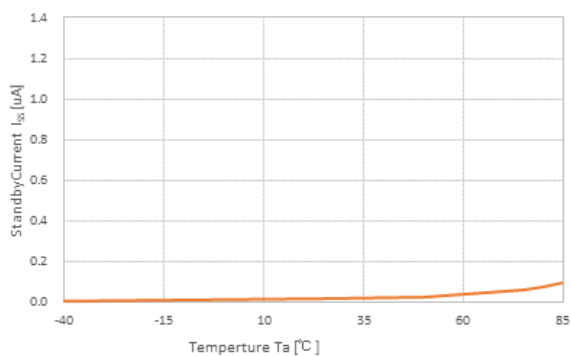
### 2) Output Current vs. Output Voltage with Different Input Voltages

RP604Z331x



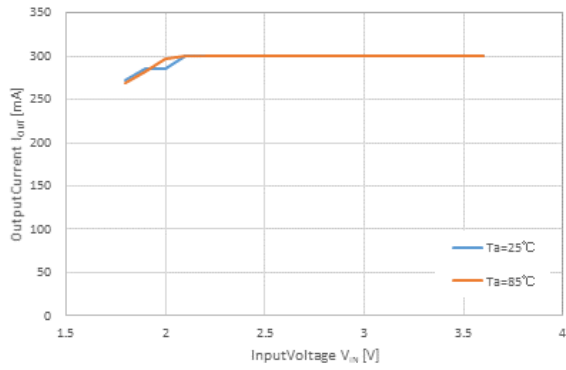
### 3) Temperature vs. Standby Current

RP604Z331x,  $V_{IN} = 5.5 V$

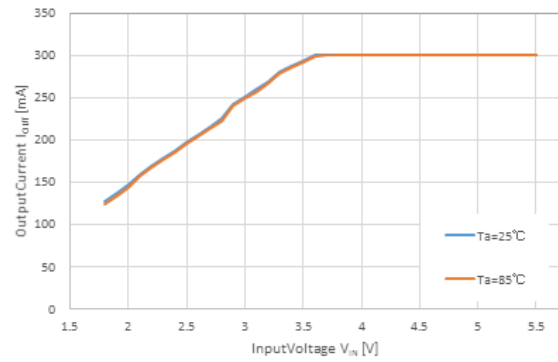


**4) Input Voltage vs. Output Current**

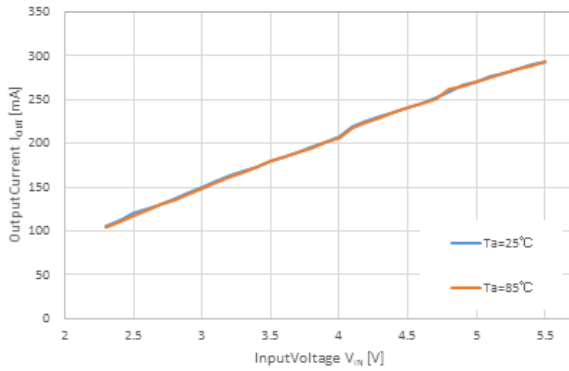
RP604Z161x,  $I_{OUT} = (I_{IN} = 300 \text{ mA})$



RP604Z331x,  $I_{OUT} = (I_{IN} = 300 \text{ mA})$

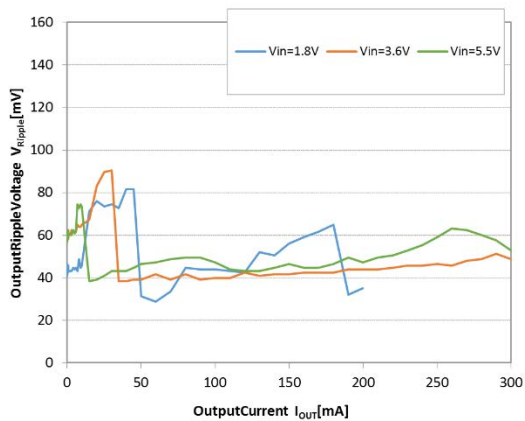


RP604Z521x,  $I_{OUT} = (I_{IN} = 300 \text{ mA})$



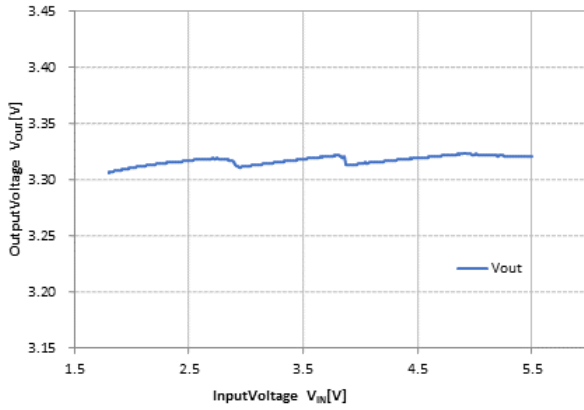
**5) Output Ripple vs. Output Current**

RP604Z331x

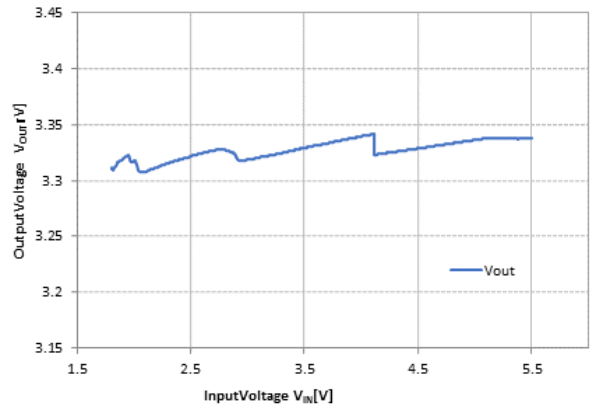


6) Input Voltage vs. Output Voltage

RP604Z331X,  $I_{OUT} = 1 \text{ mA}$

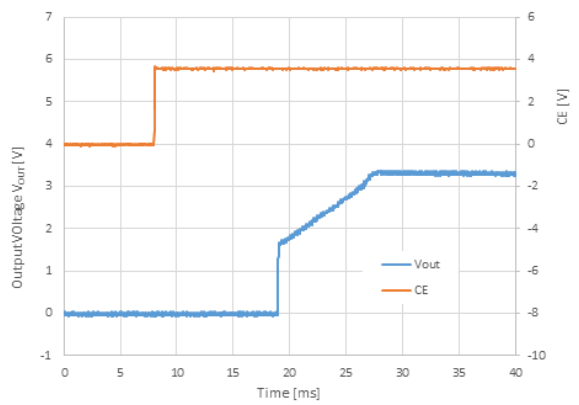


RP604Z331X,  $I_{OUT} = 100 \text{ mA}$

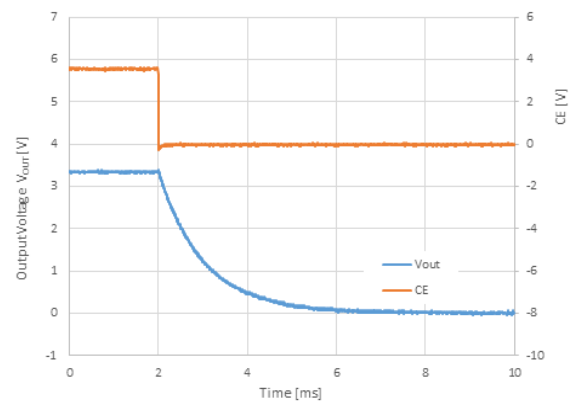


7) Starting-up/ Shutting-down Waveform with CE Pin

RP604Z331x,  $I_{OUT} = 0 \text{ mA}$

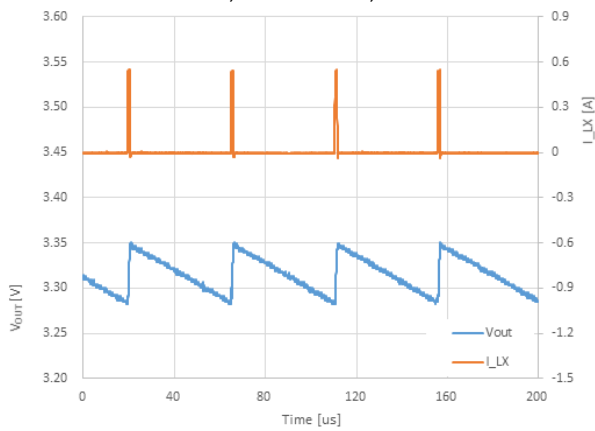


RP604Z331B,  $I_{OUT} = 0 \text{ mA}$

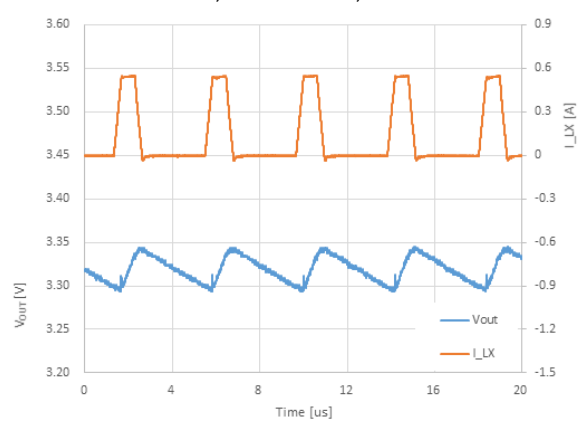


8)  $V_{OUT}$  Waveform

RP604Z331x,  $V_{IN} = 3.6 \text{ V}$ ,  $I_{OUT} = 10 \text{ mA}$

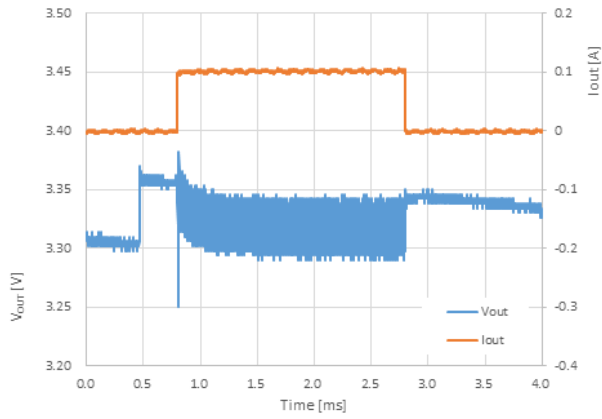


RP604Z331x,  $V_{IN} = 3.6 \text{ V}$ ,  $I_{OUT} = 100 \text{ mA}$



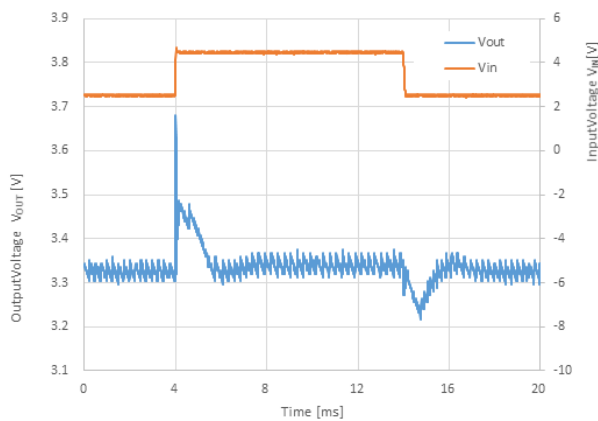
**9) Load Transient Response**

RP604Z331x,  $V_{IN} = 3.6\text{ V}$ ,  $I_{OUT} = 0.01\text{ mA} \leftrightarrow 100\text{ mA}$

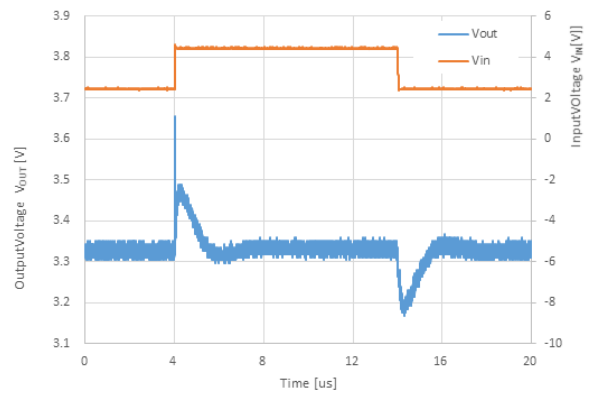


**10) Input Transient Response**

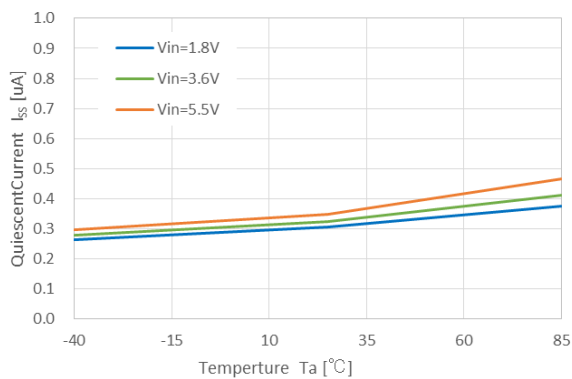
RP604Z331x,  $V_{IN} = 2.5\text{ V} \leftrightarrow 4.5\text{ V}$ ,  $I_{OUT} = 1\text{ mA}$



RP604Z331x,  $V_{IN} = 2.5\text{ V} \leftrightarrow 4.5\text{ V}$ ,  $I_{OUT} = 100\text{ mA}$



**11) Temperature vs. Supply Current**





The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-9.

**Measurement Conditions**

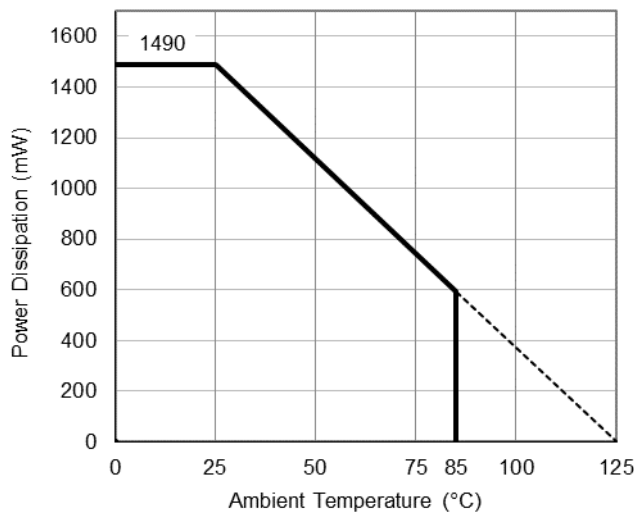
Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	101.5 mm x 114.5 mm x 1.6 mm
Copper Ratio	Outer Layers (First and Fourth Layers): 60% Inner Layers (Second and Third Layers): 100%

**Measurement Result**

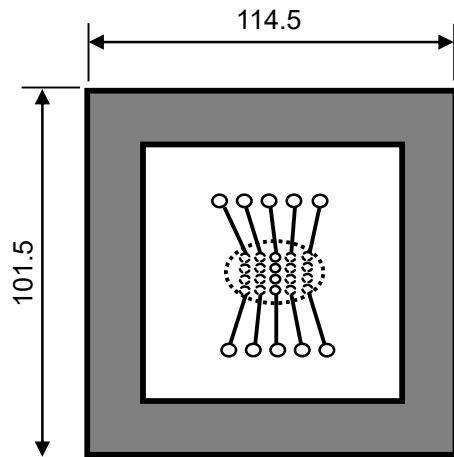
(Ta = 25°C, Tjmax = 125°C)

Item	Measurement Result
Power Dissipation	1490 mW
Thermal Resistance ( $\theta_{ja}$ )	$\theta_{ja} = 67 \text{ }^\circ\text{C/W}$

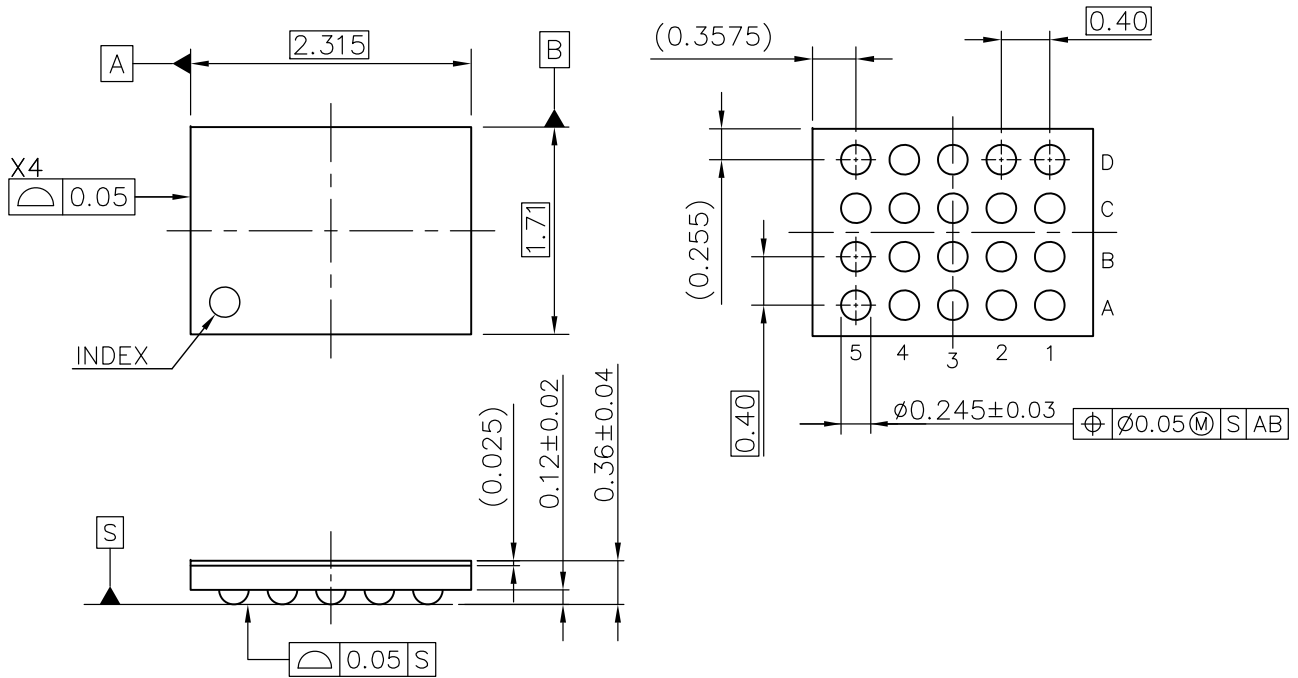
$\theta_{ja}$ : Junction-to-Ambient Thermal Resistance



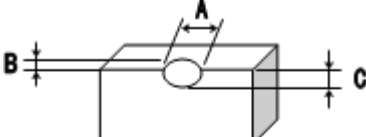
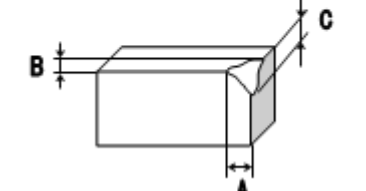
**Power Dissipation vs. Ambient Temperature**



**Measurement Board Pattern**



**WLCSP-20-P2 Package Dimensions (Unit: mm)**

No.	Inspection Items	Inspection Criteria	Figure
1	Package chipping	<p><math>A \geq 0.2\text{mm}</math> is rejected  <math>B \geq 0.2\text{mm}</math> is rejected  <math>C \geq 0.2\text{mm}</math> is rejected                      And, Package chipping to Si surface and to bump is rejected.</p>	
2	Si surface chipping	<p><math>A \geq 0.2\text{mm}</math> is rejected  <math>B \geq 0.2\text{mm}</math> is rejected  <math>C \geq 0.2\text{mm}</math> is rejected                      But, even if <math>A \geq 0.2\text{mm}</math>, <math>B \leq 0.1\text{mm}</math> is acceptable.</p>	
3	No bump	No bump is rejected.	
4	Marking miss	To reject incorrect marking, such as another product name marking or another lot No. marking.	
5	No marking	To reject no marking on the package.	
6	Reverse direction of marking	To reject reverse direction of marking character.	
7	Defective marking	To reject unreadable marking. (Microscope: X15/ White LED/ Viewed from vertical direction)	
8	Scratch	To reject unreadable marking character by scratch. (Microscope: X15/ White LED/ Viewed from vertical direction)	
9	Stain and Foreign material	To reject unreadable marking character by stain and foreign material. (Microscope: X15/ White LED/ Viewed from vertical direction)	

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

**Measurement Conditions**

Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	φ 0.3 mm × 23 pcs

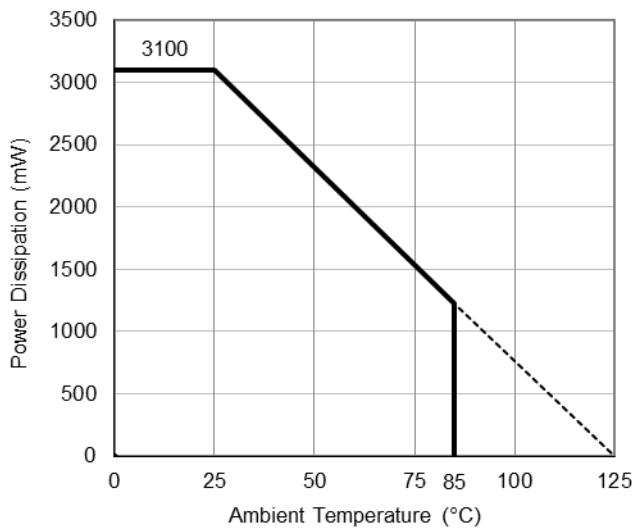
**Measurement Result**

(Ta = 25°C, Tjmax = 125°C)

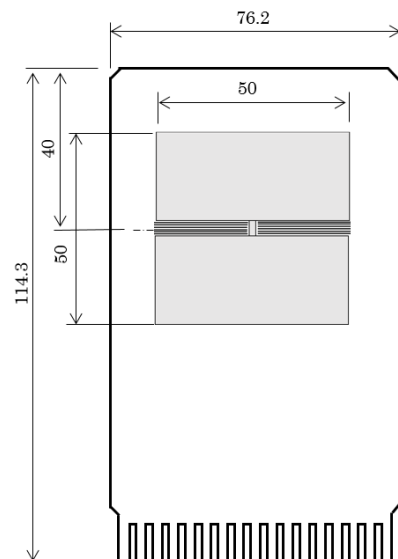
Item	Measurement Result
Power Dissipation	3100 mW
Thermal Resistance (θja)	θja = 32°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 8°C/W

θja: Junction-to-Ambient Thermal Resistance

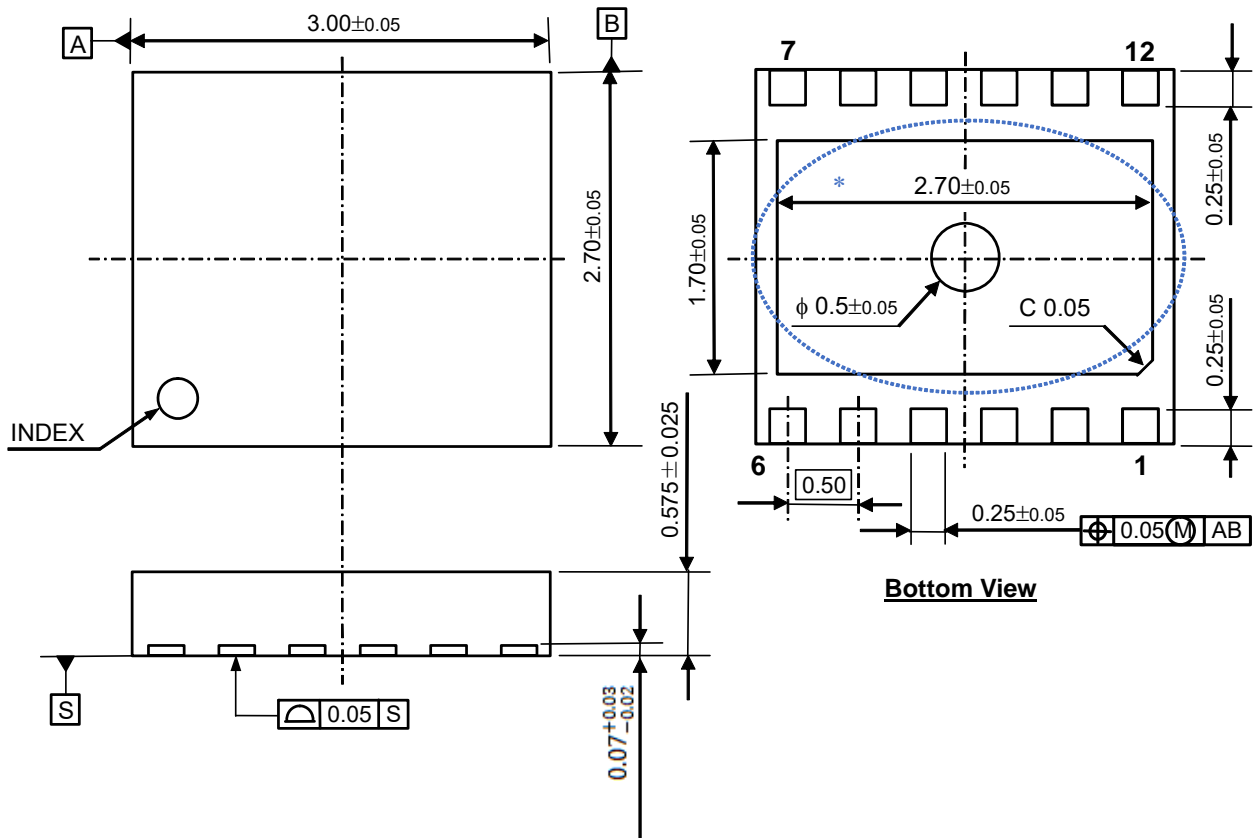
ψjt: Junction-to-Top Thermal Characterization Parameter



**Power Dissipation vs. Ambient Temperature**



**Measurement Board Pattern**



DFN(PLP)2730-12 Package Dimensions (Unit: mm)

\*The tab on the bottom of the package shown by blue circle is a substrate potential (GND). It is recommended that this tab be connected to the ground plane on the board but it is possible to leave the tab floating.



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